EE-434 Power Electronics

Engr. Dr. Hadeed Ahmed Sher

Ghulam Ishaq Khan Institute of Engineering Sciences and Technology
Topi 23460, Pakistan

hadeed@giki.edu.pk

February 27, 2020

Overview

1. DC-DC Converters
   - The BUCK converter
   - Example 6-1
   - Simulation
   - Design process
     - Design 1
     - Design 2

Introduction

Used to efficiently control the level shift in dc circuits.
Also called switch mode power supplies, switching power supplies or switchers.
Sometimes also referred as choppers.
Following properties sustain in all dc-dc converters in steady state operation.

$$i_L(t+T) = i_L(t) \tag{1}$$

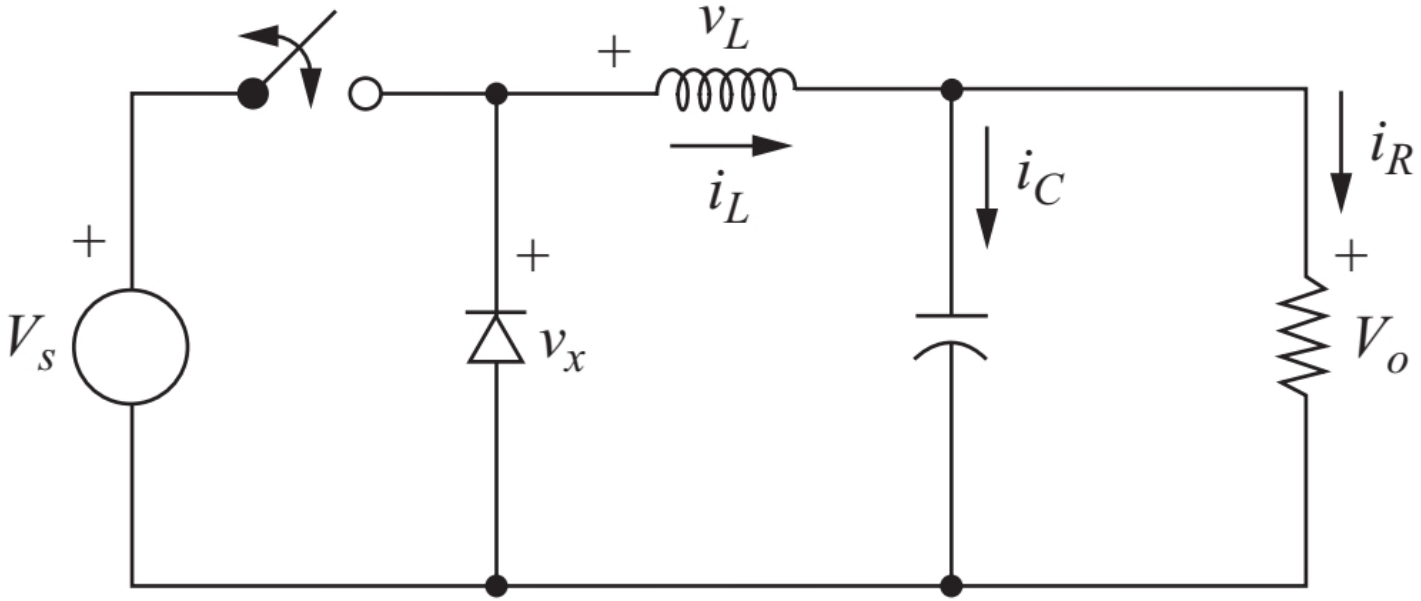
$$V_L = \frac{1}{T}\int_t^{t+T} v_L(t)dt = 0 \tag{2}$$

$$P_s = P_o \tag{3}$$

Similar expressions are valid for capacitor current.

The BUCK converter

It is used to step down the input voltage.
Figure shows the circuit of buck converter.



The converter has one controlling element, one uncontrolled element, one inductor, one capacitor and a load.
Diode is reverse biased when the switch is on and is on when switch is off.

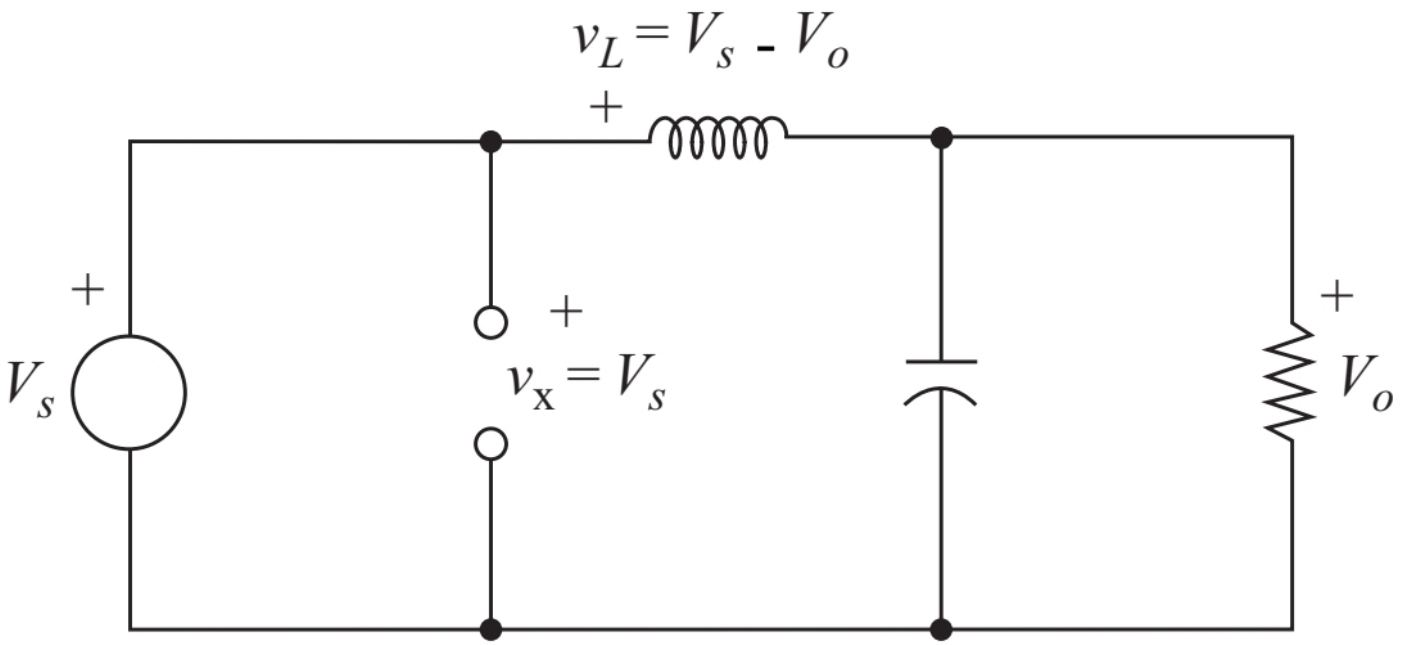
The BUCK converter

Because of the inductor in the circuit, two modes are present here i.e., CCM and DCM mode.
Analysis of such circuit can be done by examining the inductor voltage and current.
This provides useful expressions for designing inductor and capacitor.
Following assumptions are made prior to examine a buck converter

- Circuit is in steady state
- Inductor is in CCM
- Capacitor is large enough to keep the output constant.
- Switching period is divided into two parts (DT_S and (1-D)T_S)
- All components are ideal
- Circuit is analyzed with the state of controlled switch

State 1: Switch is closed

When the switch is closed the circuit of buck converter is shown below.



The diode is reverse biased because the cathode of diode is connected to the V_s.

State 1: Switch is closed

Voltage across the inductor is given as

$$v_L = V_s - V_o = L \underbrace{\frac{di_L}{dt}}_{\text{Slope}} \tag{4}$$

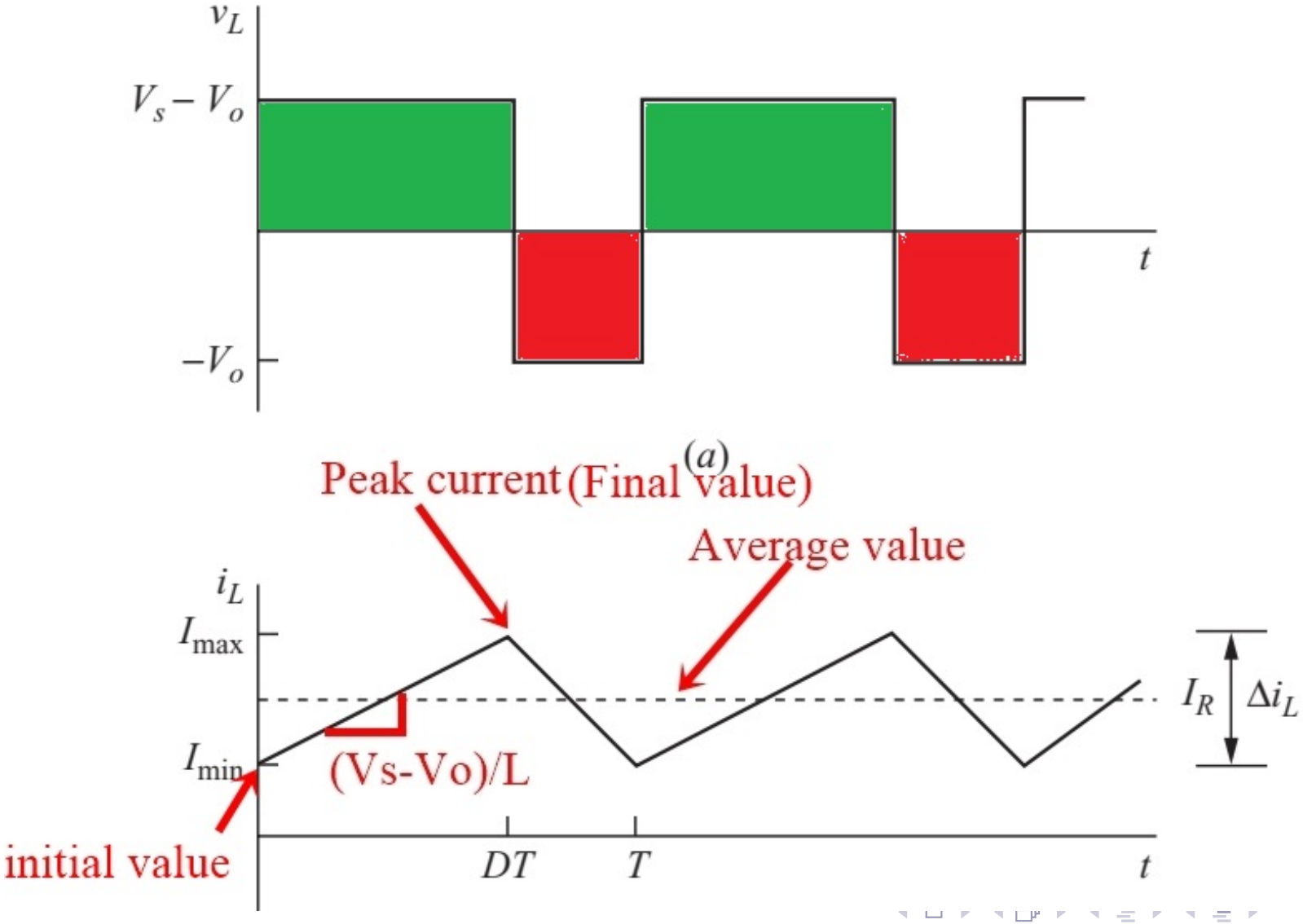
Rearranging the above expression

$$\frac{di_L}{dt} = \frac{V_s - V_o}{L} \tag{5}$$

This shows that the current rises linearly during the time, the switch is closed. Since, in this analysis the steady state condition is assumed therefore, the current shall have an initial value. During the time duration when switch is ON, the current will rise from that initial value to some final value. The time duration is shown as DT and the change in current is represented as Δi_L. It is also called current ripple.

State 1: Switch is closed

Figure shows the current waveform.



State 1: Switch is closed

The current starts from some initial value (final value of the previous switching cycle).
It increases linearly with the slope given in (5) for the entire duration of DT.
The net change in the current is equal to

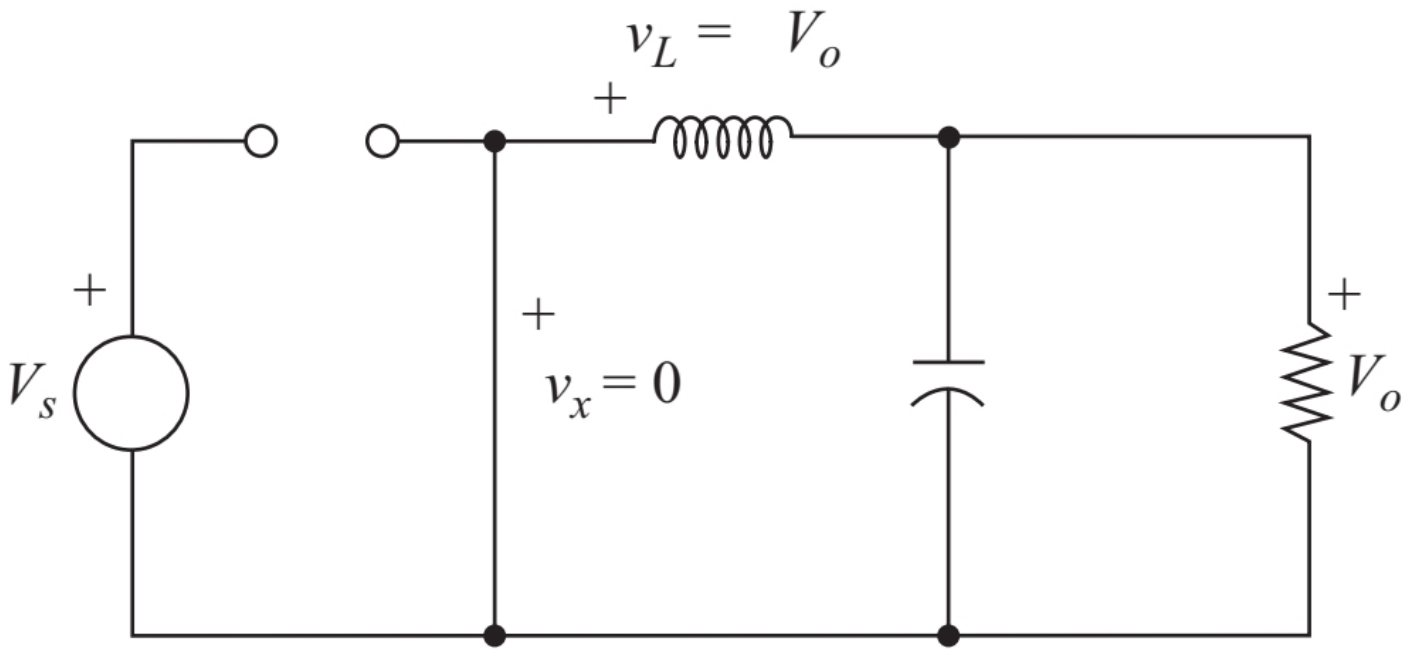
$$(\Delta i_L)_{closed} = \left(\frac{V_s - V_o}{L}\right) DT \tag{6}$$

Observations

The voltage change is instantaneous. However, current is not.

State 2: Switch is open

When the switch is open the circuit of buck converter is shown below.



The diode is forward biased to carry the inductor current.

State 2: Switch is open

Voltage across the inductor is given as

$$v_L = -V_o = L \underbrace{\frac{di_L}{dt}}_{\text{Slope}} \tag{7}$$

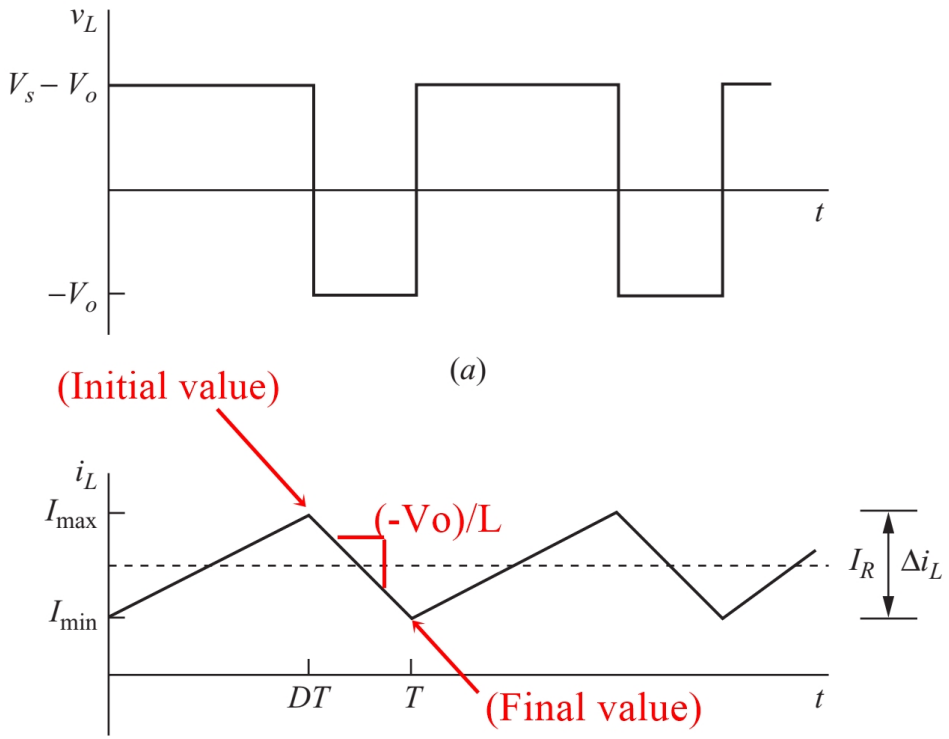
Rearranging the above expression

$$\frac{di_L}{dt} = \frac{-V_o}{L} \tag{8}$$

This shows that the current decreases linearly during this duration. The current has an initial value which is the peak value of the current during DT. During the time duration when switch is OFF, the current will fall from that initial value to some final value. The time duration is equal to (T-DT).

State 2: Switch is open

Figure shows the current waveform.



The net change in the current is equal to

$$(\Delta i_L)_{open} = \left(\frac{-V_o}{L}\right)(T - DT) \tag{9}$$

Derivation of transfer function

For steady state operation, the inductor current at the start must equals the current at the end. This means that there is no net increase or decrease in inductor current and the average inductor current is constant. It also implies that the net voltage on the inductor equals zero. Therefore, the transfer function can be obtained by the current through or the voltage across the inductor.
Using current method:

$$(\Delta i_L)_{closed} + (\Delta i_L)_{open} = 0 \tag{10}$$

Using (6) and (9),

$$\left(\frac{V_s - V_o}{L}\right)(DT) + \left(\frac{-V_o}{L}\right)(T - DT) = 0 \tag{11}$$

Solving for V_o,

$$V_o = V_s D \tag{12}$$

Derivation of transfer function

Using voltage method:

$$V_L = (V_s - V_o)DT + (-V_o)(T - DT) = 0 \tag{13}$$

This can be expressed as

$$(V_s - V_o)D - V_o(1 - D) = 0 \tag{14}$$

Solving for V_o,

$$V_o = V_s D \tag{15}$$

Observations

The output voltage is only dependent on the duty cycle and the input voltage. The output can never be greater than the input. This converter offers a linear control characteristics.

Derivation of transfer function

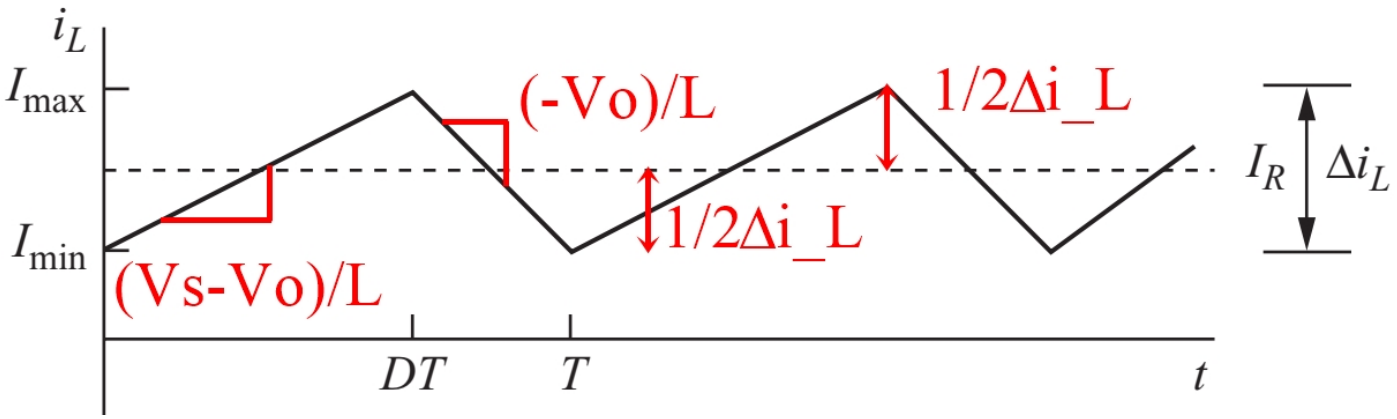
Also assuming a lossless converter

$$\begin{aligned} P_s &= P_o \\ V_s I_s &= V_o I_o \\ \frac{V_o}{V_s} &= \frac{I_s}{I_o} \end{aligned} \tag{16}$$

Eq.(16) shows that the buck converter is like a transformer. However, instead of the turn ratio, the duty cycle determine the output voltage. Moreover, it cannot stepup the input voltage.
Also, the load current is the average inductor current.

Determining the inductor value: Method 1

Figure shows the current waveform for CCM.



The fluctuation around the average value yields a minimum and a maximum value of inductor current. and because the waveform is symmetrical therefore, half of the total Δi_L is above the and half is below the average current value

$$I_{max} = I_L + \frac{\Delta i_L}{2} = \frac{V_o}{R} + \frac{1}{2}\left[\frac{V_o}{L}(1-D)T\right] = V_o\left(\frac{1}{R} + \frac{1-D}{2Lf}\right) \quad (17)$$

Determining the inductor value : Method 1

The minimum current is given as

$$I_{min} = I_L - \frac{\Delta i_L}{2} = \frac{V_o}{R} - \frac{1}{2}\left[\frac{V_o}{L}(1-D)T\right] = V_o\left(\frac{1}{R} - \frac{1-D}{2Lf}\right) \quad (18)$$

The above equation is used to determine if the circuit operates in CCM mode or in DCM mode. A zero value of I_{min} indicates the boundary between the CCM and DCM therefore , equating (18) equal to zero

$$Lf_{min} = \frac{(1-D)R}{2} \quad (19)$$

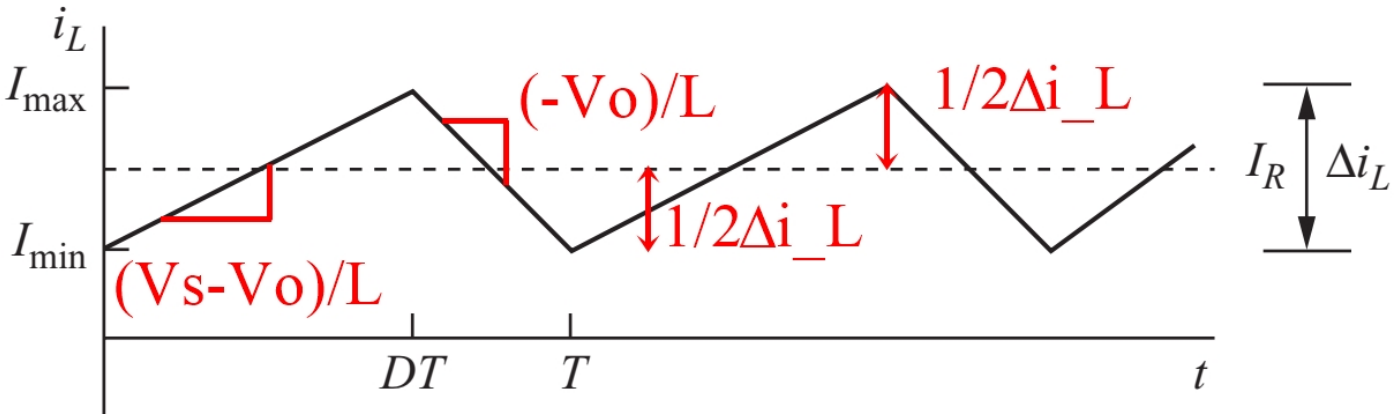
CCM mode only

$$L_{min} = \frac{(1-D)R}{2f} \quad (20)$$

Usually, a value higher then than L_{min} is selected to ensure CCM

Determining the inductor value : Method 2

Often it is desired to limit the current ripple and therefore, an expression for inductance in terms of ripple is required. To do so consider the figure shown below.



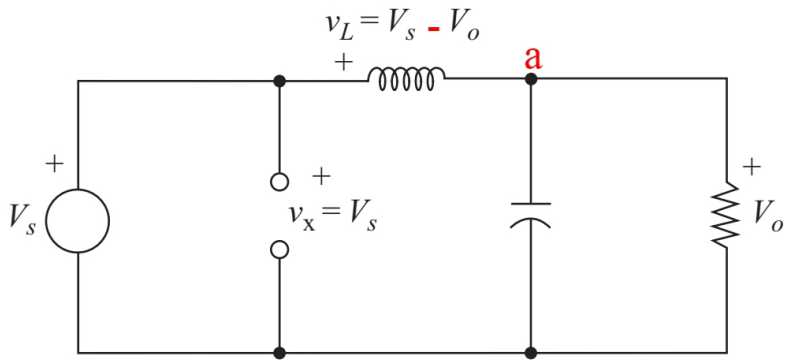
The net change in inductor current is given as

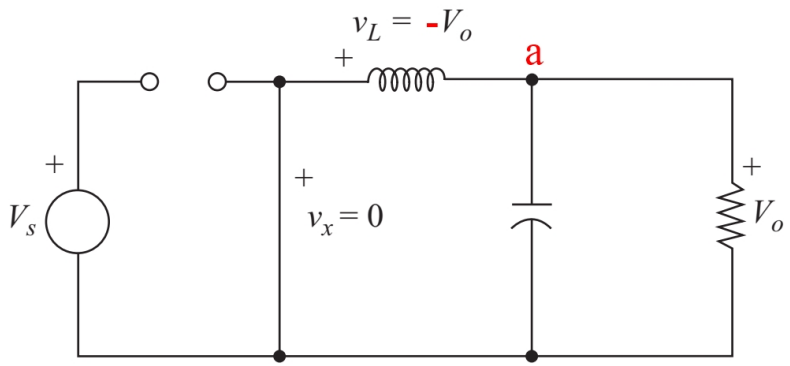
$$\Delta i_L = \left(\frac{V_s - V_o}{L}\right) DT = \underbrace{\left(\frac{V_s - V_o}{Lf}\right) D}_{\text{On time}} = \underbrace{\frac{V_o(1-D)}{Lf}}_{\text{Off time}} \tag{21}$$

$$L = \left(\frac{V_s - V_o}{\Delta i_L f}\right) D = \frac{V_o(1-D)}{\Delta i_L f} \tag{22}$$

Determining the capacitor value

The capacitor current waveform is required to determine the capacitor. So, the capacitor current is analyzed for the switch On and OFF state. Consider the following circuit.





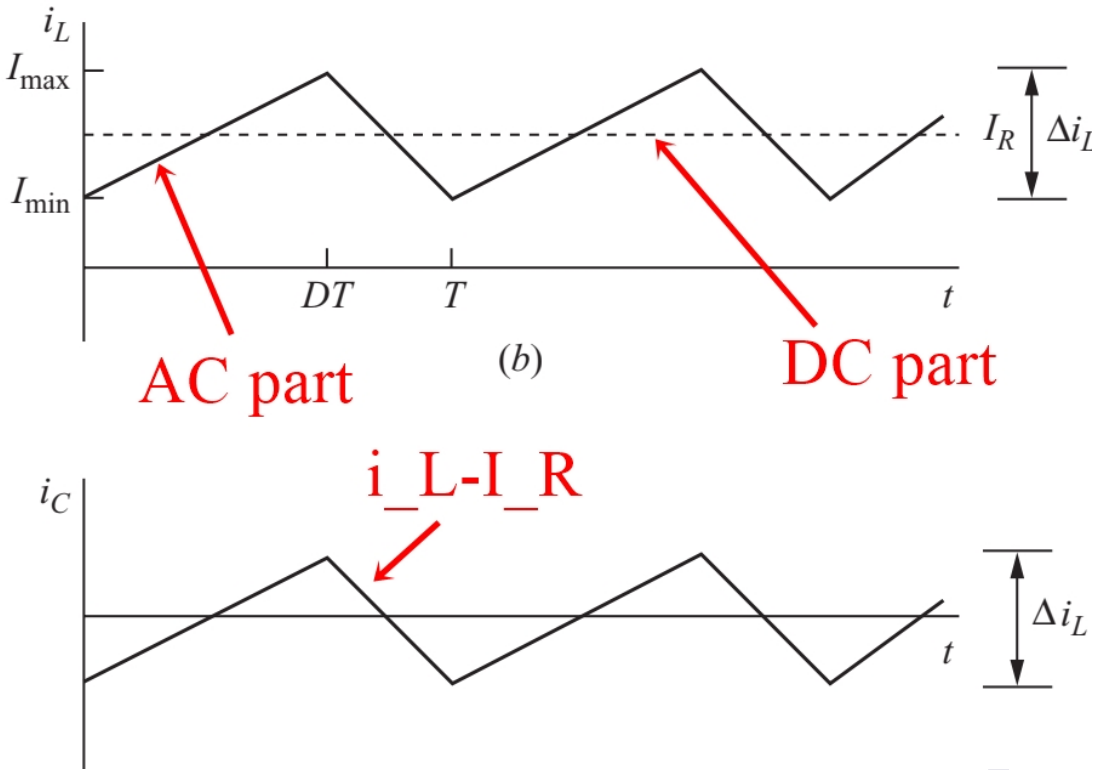
Apply KCL at node 'a' for both circuits.

$$i_C = i_L - i_R \tag{23}$$

When the capacitor current is positive, the capacitor is charging and it is discharging with a negative value. The current through a capacitor should have a zero net value for a steady state condition.

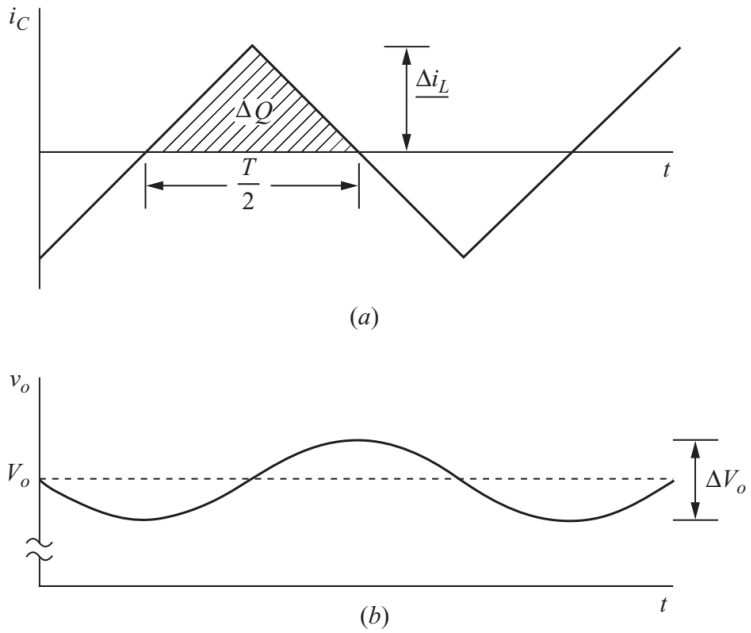
Determining the capacitor value

The inductor current has a rising and falling slopes with a fixed average (dc) value. That average value cannot pass through the capacitor (Hint:X_c). Thus, the average component of the inductor current passes through the load and the ac component comes into the capacitor. Therefore, capacitor current waveform is actually a subtraction of inductor current with its average value.



Determining the capacitor value

Consider a more expounded view of Fig.20



Using Q=CV,

$$\Delta Q = C\Delta V_o \implies \Delta V_o = \frac{\Delta Q}{C} \tag{24}$$

Determining the capacitor value

The change in charge is the area of the triangle above time axis. Using Q=CV,

$$\Delta Q = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{T\Delta i_L}{8} \tag{25}$$

This results in

$$\Delta V_o = \frac{T\Delta i_L}{8C} \tag{26}$$

Since the capacitor is connected at the output, using (9) here

$$\Delta V_o = \frac{TV_o}{8CL}(1-D)T = \frac{V_o(1-D)}{8LCf^2} \tag{27}$$

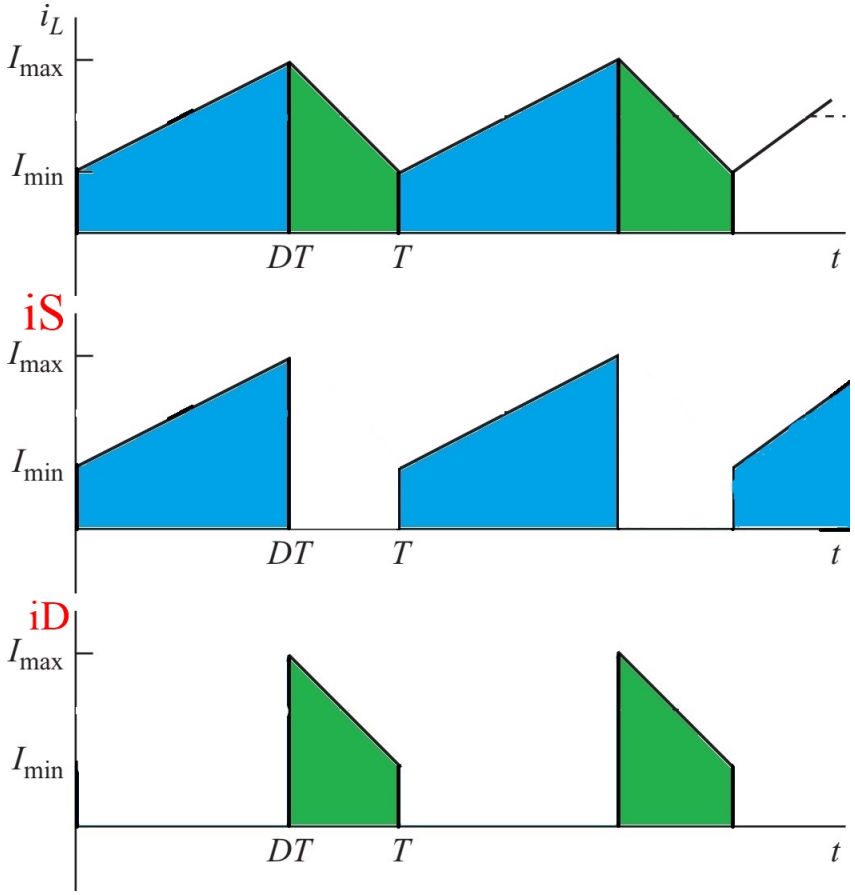
$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8CLf^2} \tag{28}$$

Thus, the capacitor value can be calculated as

$$C = \frac{1-D}{8L(\Delta V_o/V_o)f^2} \tag{29}$$

Currents in buck converter

When switch is ON, the switch current is the same as inductor current. The switch should be able to withstand the maximum current. Diode current is zero. When switch is OFF, the switch current is zero, the diode current is equal to the inductor current.



What happens when the converter starts?

When the converter is first turned on, the capacitor is uncharged and so is the inductor.

$$i_L(0^-) = i_L(0^+) = 0A \tag{30}$$

During first sub interval the switch is on and hence inductor current will rise linearly given as

$$i_L = \frac{V_s - V_o}{L} \tag{31}$$

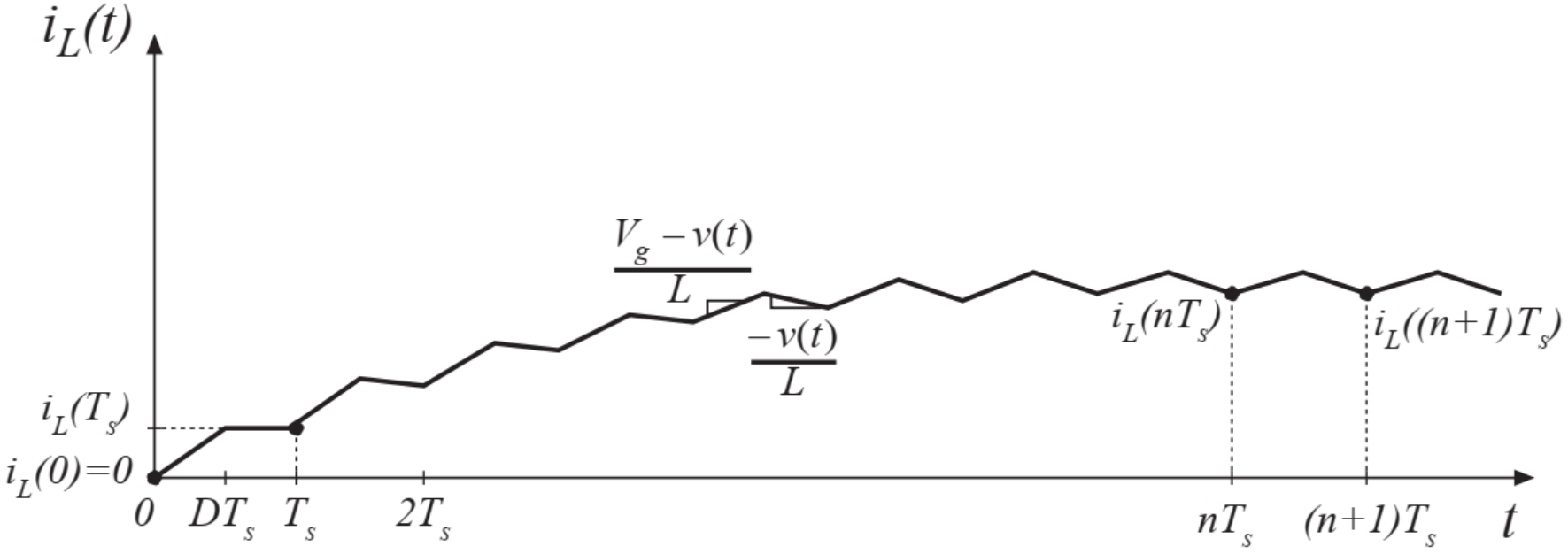
Since V_o is zero (assuming C uncharged). The slope of inductor current is essentially $\frac{V_s}{L}$.
During second sub interval the switch is off and therefore, the slope of inductor current is

$$i_L = \frac{-V_o}{L} \tag{32}$$

Since, the output voltage is zero, the slope is essentially zero during this time.

What happens when the converter starts?

Off course during the first sub interval the current passes through the output capacitor and therefore, voltage will appear across the capacitor. But because the switching times are very high, the voltage on capacitor is assumed negligible for the second sub interval.
Also, during the first switching cycle there is a net increase in inductor current. Next switching cycle will increase the capacitor voltage and the system continues until the equilibrium state is reached.



Example 6-1

The buck dc-dc converter has the following parameters: Vs=50 V, D=0.4, L=400 μH,C=100μF,f=20 kHz, R=20ω Assuming ideal components and CCM , calculate (a) the output voltage V_o, (b) the maximum and minimum inductor current, and (c) the output voltage ripple.

Solution :

(a) Using (15) V_o=20V

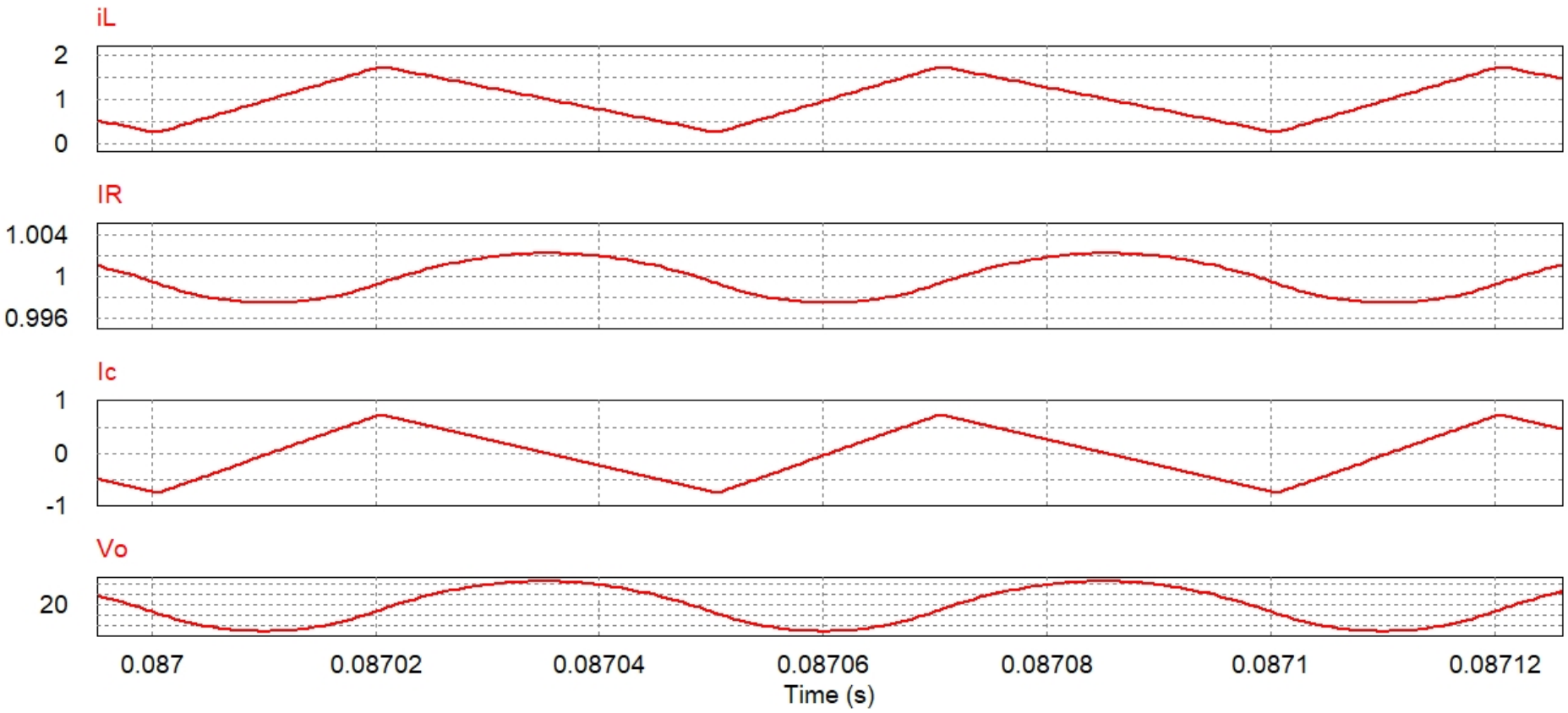
(b) Using (17) and (18) I_{max}=1.75A and I_{min}=0.25A.

Note that minimum current is positive , thus validating CCM.

(c) Using (28) output voltage ripple is 0.469%.

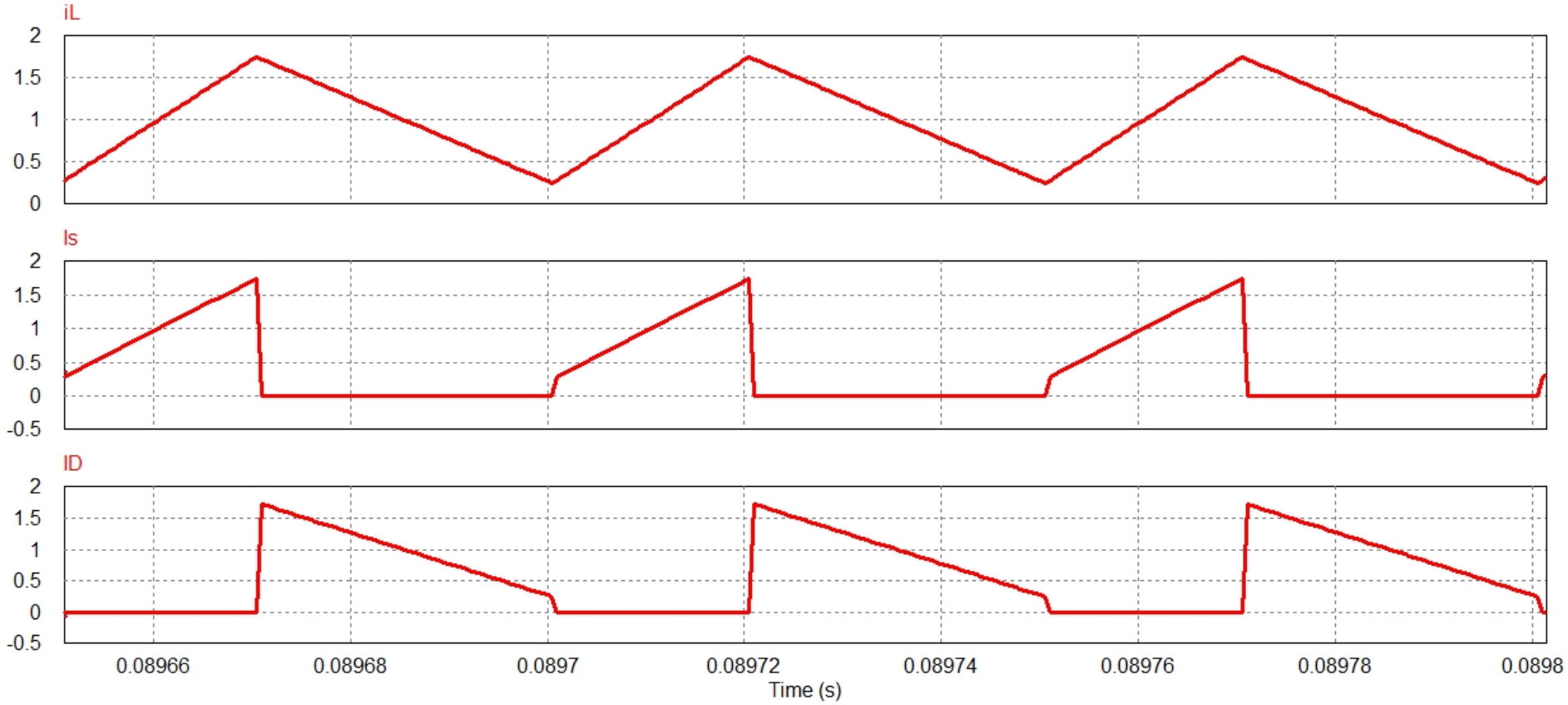
Simulation of Example 6-1

iL is the inductor current, IR is the load current, Ic represents capacitor current and Vo is the output voltage



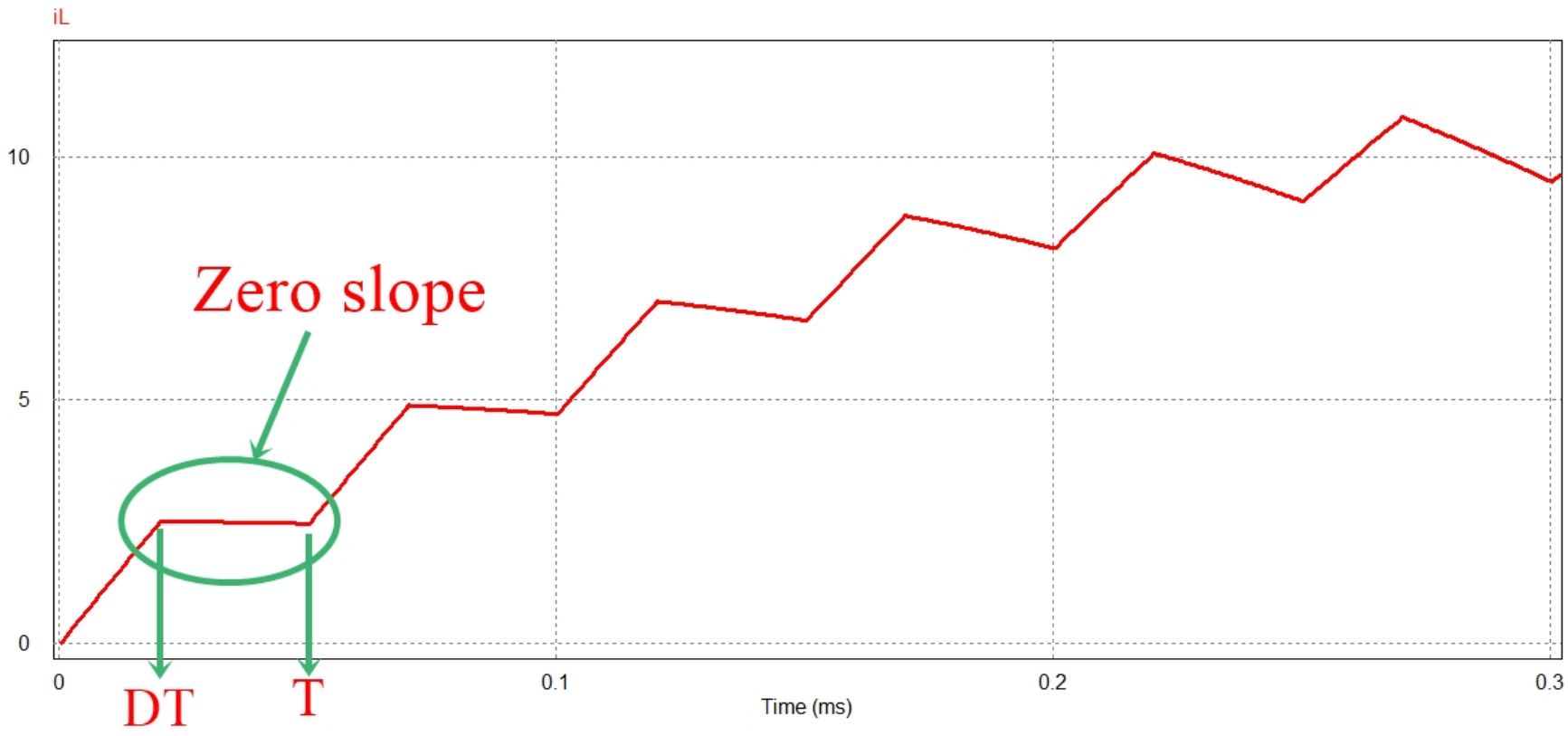
Simulation of Example 6-1

iL is inductor current. Is is the current through the switch and ID is the diode current.



Simulation of Example 6-1

Inductor current during first switching instant.



Design process

Following are some important design considerations

- Usually designed for CCM
- Usually inductor value is 25% larger than the minimum value calculated.
- Larger the inductor is, smaller is the ripple current. Sometimes designers specify upto 40% the ripple current to keep the inductor small.
- Inductor wire is rated at rms current and the core is selected such that it do not saturate at peak inductor current.
- Capacitor is selected on the bases is of output ripple. Usually 5-10% ripple is desired .Eq.(19) and (22) are frequently used
- Switching frequency is usually kept high to reduce the size of filter elements.
- Higher switching frequencies create switching losses and requires larger heat sinks.
- Optimization is required for selecting the switching frequency.

Design process

- Usually switching frequencies are selected higher than 20kHZ to avoid audible noise.
- Switching frequencies are as high as in MHz. It is purely a designer perspective and choice.
- For low voltage high current applications, synchronous rectification scheme is deployed.
- MOSFET with low R_{DSon} is desired.
- MOSFET and Diode are selected according to the switching frequency.
- A low t_{rr} diode is required.
- The MOSFET and diode must withstand maximum voltage stress when off and peak current when on.
- Heat sink design is mostly require for a safe operation.
- Protection should be included in the circuit to avoid any fatal accident.

Buck converter design 1. Example 6.2

Scenario

Design a buck converter in CCM to produce an output voltage of 18 V across a 10-Ω load resistor using 48V supply. The output voltage ripple must not exceed 0.5%. Specify the D, the switching frequency, the values of the inductor and capacitor, the peak voltage rating of each device, and the rms current in the inductor and capacitor. Assume ideal components.

Solution:
Using (12) D=$\frac{V_o}{V_s} = 0.375$.
Assume a frequency of 40kHz.
Minimum inductor value is calculated using (20). $L_{min} = \frac{(1-D)R}{2f}$=78$\mu$H.
Using the guidelines provided on slide 30, the inductance is chosen as L=1.25L_{min}=97.5μH.
Maximum and minimum current through inductor is given in (17) and (18). $I_{max} = I_L + \frac{\Delta i_L}{2}$ and $I_{min} = I_L - \frac{\Delta i_L}{2}$

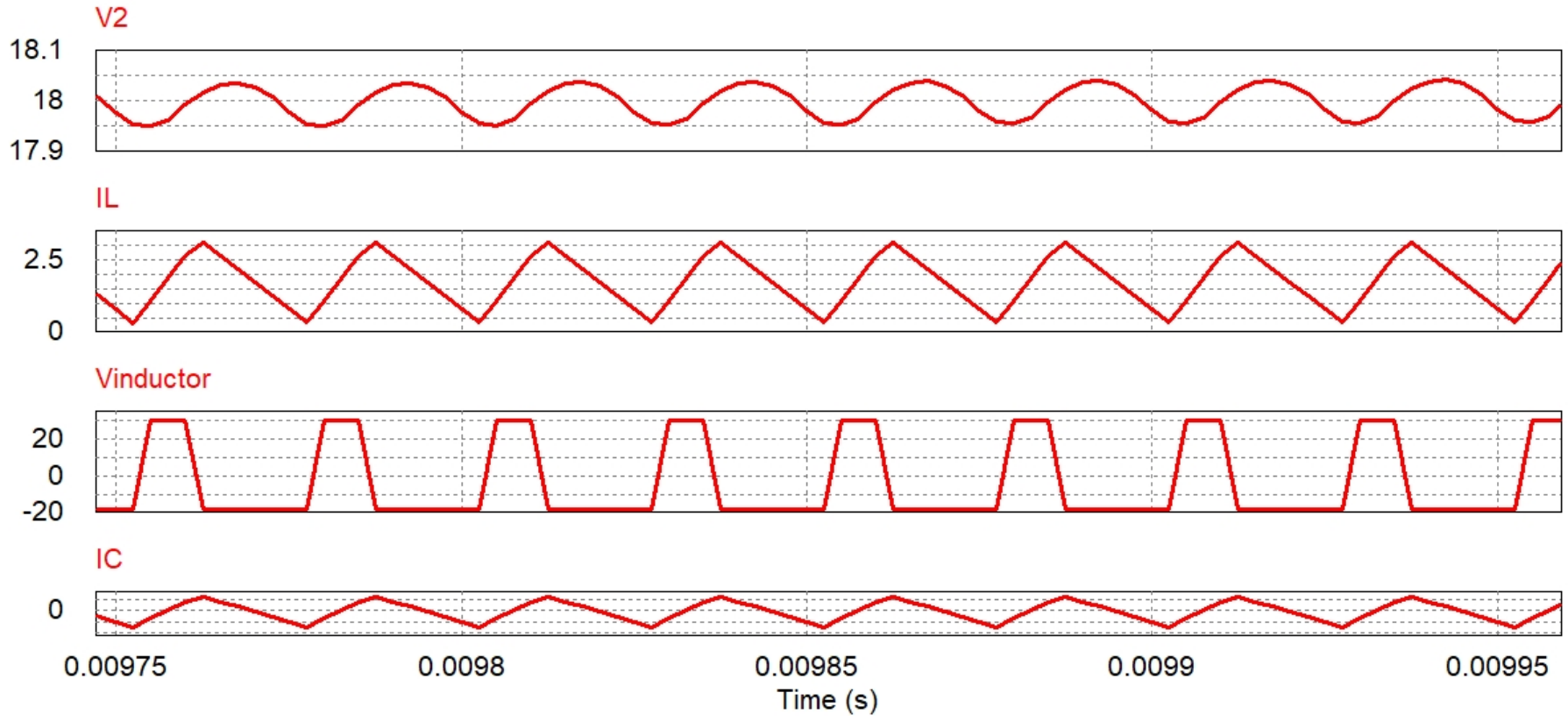
Buck converter design 1. Example 6.2

Now, I_L is the average value that flows only through load. It is calculated as $I_L = \frac{V_o}{R} = 1.8A$.
Using (21), $\Delta i_L = (\frac{V_s - V_o}{L})DT$=2.88A.
Therefore, $I_{max} = 1.8 + 1.44 = 3.24A$ and $I_{min} = 1.8 - 1.44 = 0.36A$
Inductor is rated for rms current. For an offset triangular waveform

$$I_{L,rms} = \sqrt{I_L^2 + \left(\frac{\Delta i_L/2}{\sqrt{3}}\right)^2} = 1.98A \tag{33}$$

Capacitor is calculated using (29), $C = \frac{1-D}{8L(\Delta V_o/V_o)f^2}$=100$\mu$F.
Peak capacitor current is $\Delta i_L/2$=1.44A and rms capacitor current for triangular waveform is $1.44/\sqrt{3}$=0.83A.
Maximum voltage across switch and diode is V_s. Inductor voltage when switch is ON is 48-18=30V and when OFF is 18V. So inductor must withstand 30V. Capacitor must be rated for 18V output.

Simulation results of design problem 1



V2 is the output voltage.Notice the ripple component. IL is the inductor current. Vinductor is voltage across inductor and IC is the capacitor current. All match the calculated values.

Buck converter design 2. Example 6.3

Scenario

Power supplies for telecommunications applications may require high currents at low voltages. Design a buck converter that has an input voltage of 3.3 V and an output voltage of 1.2 V. The output current varies between 4 and 6 A. The output voltage ripple must not exceed 2%. Specify the inductor value such that the peak-to-peak variation in inductor current does not exceed 40% of the average value. Determine the required rms current rating of the inductor and of the capacitor. Determine the maximum equivalent series resistance of the capacitor.

Solution:
Concept of synchronous rectification is required here.
Using (12) D=0.364.
Let switching frequency be 500kHz

Buck converter design 2. Example 6.3

Average inductor current is same as output current. Analyzing for 4A output.

$$I_L = I_o = 4A \implies \Delta i_L = (40\%)(4) = 1.6A \tag{34}$$

Using (22) L=9.55μH.
Repeating this procedure for 6A output current L=0.636μH.
Larger value of inductance is chosen. Inductor rms current is calculated using (33) . Also using (21) the variation in inductor current is 1.6A.
Using 6A output, inductor must be rated for an rms current of 6.02A.
Using L=1μH the C is determined as 0.16μF.
If the capacitor is assumed non-ideal then

$$\Delta V_o \approx r_C \Delta i_C = r_C \Delta i_L \tag{35}$$

so r_C which is ESR is equal to 15mΩ. So from data sheet chose the capacitor with this value of ESR. Peak capacitor current is $\Delta i_L/2$=0.8A and rms capacitor current for a triangular waveform is $0.8/\sqrt{3}$=0.46A